

Patent Claims

1. Circuit arrangement for receiving data that are allocated to at least one time slot (TS1, TSn, TSn+x, ...) within a transmission frame, comprising
 - a first processing unit (WSPE) for readout of the data out from a current time slot (TSn) and offering the current state parameters of the current time slot (TSn), for intermediately storing the state parameters of a time slot (TSn+x) following the current time slot (TSn), and for intermediately storing the readout data of a time slot (TSn) in a first memory unit (SE);
 - a second processing unit (BV) with an allocation unit (ZU) for administering a second memory unit (ST) in which state parameters read from the first memory unit (SE) given a time slot change are stored, for editing the state parameters intermediately stored in the first memory unit (SE), and for allocation of the data of a current time slot (TSn) intermediately stored in the first memory unit (SE) into a third memory unit (EQ); and
 - a third processing unit (FV) for forming data words from the data deposited in the third memory unit (EQ).
2. Circuit arrangement for transmitting data that are allocated to at least one time slot (TS1, TSn, TSn+x, ...) within a transmission frame, comprising
 - a first processing unit (WPSS) that comprises a unit (P/S) for reading the data in a current time slot (TSn) into the transmission frame and offering the current state parameters for a current time slot, and a first memory unit (SS) for intermediately storing the state parameters of a time slot (TSn+x) following the current time slot (TSn);
 - a second processing unit (BVS) with an allocation unit (ZU) for administering a second memory unit (STS) in which state parameters read from the first memory unit (SS) given a time slot change are stored, for editing the state parameters to be intermediately stored in the first memory unit (SS), and for allocation of the data intermediately stored in a third memory unit (DTS) into the first memory unit (SS); and

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unit (SS), and for allocation of the data intermediately stored in a third memory unit (DTS) into the first memory unit (SS); and
 – a third processing unit (FVS) for the allocation of data belonging to time slots (TS_n , TS_{n+x}) and their storing in a third memory unit (DTS).

5 6. Method for the reception of data that are arranged in a transmission frame, whereby different time slot widths on the same transmission link can be configured within the transmission frame,

- that data from a current time slot (TS_n) are read out and intermediately stored and current state parameters of the current time slot are offered and
 10 state parameters of a time slot (TS_{n+1}) following the current time slot (TS_n) are intermediately stored in a first memory unit (SE);
- that [...] in a second memory unit (ST) in which state parameters read from the first memory unit (SE) given a time slot change are stored and administered;
- 15 – that state parameters to be intermediately stored in the first memory unit (SE) are offered and data of a current time slot (TS_n) to be intermediately stored in the first memory unit (SE) are read into a third memory unit (EQ); and
- that data words are formed from the data deposited in the third memory
 20 unit (EQ).

7. Method for the transmission of data that are arranged in a transmission frame, whereby different time slot widths on the same transmission link can be configured within the transmission frame,

- that state parameters of a current time slot are offered and data are read
 25 into a current time slot (TS_n), and state parameters of a time slot (TS_{n+1}) following the current time slot (TS_n) are intermediately stored in a first memory unit (SS);
- that the state parameters to be intermediately stored in the first memory unit (SS) are offered in a second memory unit (STS) in which state
 30 parameters read from the first memory unit (SS) given a time slot change

following the current time slot (TS_n) are intermediately stored in a first memory unit (SS);

- the state parameters to be intermediately stored in the first memory unit (SS) are offered in a second memory unit (STS) in which state parameters read from the first memory unit (SS) given a time slot change are stored, and the data intermediately stored in a third memory unit (DTS) [...] the first memory unit (SS);
- data belonging to time slots (TS_n , TS_{n+x}) are allocated and their storing in the third memory unit (DTS) are stored. [SIC!!!]

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